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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,459	11/20/2003	Atsushi Nakamura	HITA.0463	6842

38327 7590 06/15/2007

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EXAMINER	
PRENDERGAST, ROBERTA D	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
06/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,459	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Roberta Prendergast	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5 and 8-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5 and 8-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 8- and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,850,224 to Sakuraba, U.S. Patent No. 6,005,572 to Kurihara, and U.S. Patent No. 5,657,478 to Recker et al.

As per claim 1, Sakuraba teaches in Fig. 3, Fig. 9, Fig. 47, and col. 14 lines 51-57 a 3-dimensional drawing apparatus comprising a plurality of frame buffers storing separate display planes that are superimposed together as a single display output. The apparatus includes a 3-dimensional drawing mechanism 22 which is comprised of a plurality of parallel drawing processing units 32 and a frame memory 34 for a plurality of display planes. The drawing processing units 32 receive 3-dimensional image data consisting of instructions to calculate the coordinate transformations and color values for vertexes of a polygon. The drawing units execute these pixel interpolations in parallel and store the resulting image data in areas of a frame memory prepared for a plurality of pictures planes. In the embodiment shown in Fig. 50, there are a plurality of frame memories 422, 424, and 426 responsible for storing display plane image data and superimposed image data. From the claim, the image data is generated according to a

series of data. Although Sakuraba does not explicitly state that the image data is processed for the display planes according to a series of data, it can be assumed for obvious reasons that there are instructions provided to store the display face image data in their respective frame memory locations. In order for the claimed apparatus to optimally perform display plane switching, a CPU would be needed to provide instructions that facilitate data transfer from the image generating unit to the frame memories. Sakuraba teaches in Fig. 49 and col. 27 lines 32-58 a display control section 428 ("display processing circuit") that reads out the synthesized ("superimposed") image from the frame memory and converts it into analog output signals for display. The display control section 428 does not superimpose the image data as in the claimed display processing circuit, however, Sakuraba teaches in Fig. 47 and col. 25 lines 49-54 a depth data control mechanism 24-1, 24-2, and 24-3 which synthesizes the picture planes according to the depth coordinate z values associated with each pixel. As shown in Fig. 9, the synthesized image data is transferred via transfer buffer 36 to the display frame memory 38, where it is read out by the display control section 40 (col. 26 lines 54-58). It is noted that although two separate display control section embodiments 40 and 428 for the 2-dimensional and 3-dimensional drawing mechanisms respectively are referenced, both read the synthesized image from the frame memory for analog display output. Sakuraba teaches in Fig. 50 and col. 29 lines 44-52 a frame control section 435 within the 3-dimensional drawing mechanism that can switch and select from which frame buffer to read the image data so that it can be superimposed ("storage areas...are capable of switching for each display face"). The frame control section 435

superimposes the image data from the frame buffers by selecting a frame buffer based on the comparison of the per-pixel depth data z values for the image data and writing to a display frame buffer. The image data corresponding the smaller Z value is written. Rather than implementing this switching functionality within the display control section as is in the claimed display processing circuit, Sakuraba implements it within the frame control section. Doing so does not considerably alter the functionality of the apparatus because in both cases, frame buffers are written to and data is superimposed, in that order. However, it would have been obvious to one of ordinary skill in the art at the time to implement both the switching and superimposing functionality within the display control section in order to eliminate the time associated with switching between the frame buffers, writing the superimposed image data to another frame memory, and then reading the image data out as analog output signals. By superimposing the image data and directly converting it to analog output signals within the display control section, there is no need to temporarily store the superimposed image data, thus reducing the time required to superimpose and display image data.

Kurihara discloses a double buffering display unit comprising of a CPU 21, a frame buffer control circuit 25, a mask plane 41, and two frame buffers 22 and 23 corresponding to display planes A and B respectively. With conventional double buffering, image data is stored in the first and second buffers and a display controller reads from one buffer or the other. However, Kurihara teaches in col. 4 lines 22-25 an additional mask plane storing 1-bit data per pixel indicating whether the associated image data is located in the first or second frame buffer ("setting is made whether or not

a storage area from which the image data is read is switched for each display face"). By initially storing which frame buffer the image data is stored in, the time required to transfer this image data to a display frame buffer is reduced because the location (first or second frame buffer) of this image data does not have to be determined. In Fig. 9, Kurihara teaches that after image data is read and written into a frame buffer (S62, S64) according to the new screen coordinates set in S42-S46, 1-bit pixel data is read from and written to the mask plane according to the pixel's start and destination coordinates (S66) ("setting made...at termination of generation of image data"). Kurihara teaches in Fig. 2A, Fig. 2C, col. 5 lines 4-46 that the control register 26 ("a first register") included within the frame buffer control circuit 26 is used to store the control bits (b1 b0) ("display enable bits") indicating the frame buffer or mask plane to be accessed. A control signal based on the control bits is then output to the frame buffers via control bus 36 and 42 ("setting of switching...is performed based on the display switching enable bits"). Kurihara does not expressly teach a one-to-one correspondence between each of the control bits ("display enable bits") and a display face. However, the control bits serve as operation codes for switching to the frame buffers and mask plane. In Fig. 9, Kurihara teaches that the process of controlling the frame buffers in order to generate new image data for output consists of setting the control bits in the control registers (S61, S63, S65) and reading and writing image data into the frame buffers on a per-pixel basis. The figure illustrates with S61 and S63 that after setting the control bits in the control register corresponds to switching to either the first or second frame buffer ("setting of switching to a storage area...is performed by updating the first register").

Recker teaches in col. 5 lines 7-31 that the co-processor instructs the display controller 60 to switch between alternate frame buffers in order to avoid performance bottlenecks at the host processor and to prevent tearing of the displayed image. Recker teaches that the command to switch frame buffers does not necessarily have to be synchronized with the display timing. However, the subsequent display instructions are buffered while waiting for the frame buffers to switch so that they can be executed with the next vertical retrace. This double buffering alleviates the situation when a host processor cannot maintain the data transfer necessary for smooth video output. The host processor always writes to one buffer and a display controller always reads the other buffer. It is necessary for the frame buffers to be switched in synchronization to the vertical retrace so that a completely drawn image is displayed each time a frame buffer switch occurs thus indicating that the V_FIFO_SYNC_AND_RESPOND command/signal indicates whether or not the storage area, i.e. frame buffer, from which the area to be read is switched.

Therefore it would have been obvious to replace Sakuraba's depth data control mechanism for determining which frame buffer to access with Kurihara's method and apparatus so that data stored in the frame buffers can be quickly transferred to a display frame buffer without having to spend time determining from a Z buffer which frame buffer the image data should be retrieved from because Kurihara's method and apparatus provides a way of initially storing an indication of which frame buffer image data is stored in. Further, it would have been obvious to one of ordinary skill in the art at the time to incorporate Reckers' method of switching the frame buffers in sync with the

display vertical synchronization signal with the combined teachings of Sakuraba and Kurihara in order to create a display controller that can quickly transfer the data stored in the frame buffers to a display frame buffer and can display images without tearing or flickering.

As per claims 3-4, Sakuraba teaches the switching of frame buffers is determined by comparing the depth data z values, but Sakuraba fails to expressly teach of a setting made to indicate whether or not a storage area is to be switched.

Kurihara discloses a double buffering display unit comprising of a CPU 21, a frame buffer control circuit 25, a mask plane 41, and two frame buffers 22 and 23 corresponding to display planes A and B respectively. With conventional double buffering, image data is stored in the first and second buffers and a display controller reads from one buffer or the other. However, Kurihara teaches in col. 4 lines 22-25 an additional mask plane storing 1-bit data per pixel indicating whether the associated image data is located in the first or second frame buffer ("setting is made whether or not a storage area from which the image data is read is switched for each display face"). By initially storing which frame buffer the image data is stored in, the time required to transfer this image data to a display frame buffer is reduced because the location (first or second frame buffer) of this image data does not have to be determined. In Fig. 9, Kurihara teaches that after image data is read and written into a frame buffer (S62, S64) according to the new screen coordinates set in S42-S46, 1-bit pixel data is read from and written to the mask plane according to the pixel's start and destination coordinates (S66) ("setting made...at termination of generation of image data"). Kurihara teaches in

Fig. 2A, Fig. 2C, col. 5 lines 4-46 that the control register 26 ("a first register") included within the frame buffer control circuit 26 is used to store the control bits (b1 b0) ("display enable bits") indicating the frame buffer or mask plane to be accessed. A control signal based on the control bits is then output to the frame buffers via control bus 36 and 42 ("setting of switching...is performed based on the display switching enable bits"). Kurihara does not expressly teach a one-to-one correspondence between each of the control bits ("display enable bits") and a display face. However, the control bits serve as operation codes for switching to the frame buffers and mask plane. In Fig. 9, Kurihara teaches that the process of controlling the frame buffers in order to generate new image data for output consists of setting the control bits in the control registers (S61, S63, S65) and reading and writing image data into the frame buffers on a per-pixel basis. The figure illustrates with S61 and S63 that after setting the control bits in the control register corresponds to switching to either the first or second frame buffer ("setting of switching to a storage area...is performed by updating the first register"). Kurihara's method and apparatus provides a way of initially storing an indication of which frame buffer image data is stored in.

It would have been obvious to replace Sakuraba's depth data control mechanism for determining which frame buffer to access with Kurihara's method and apparatus so that data stored in the frame buffers can be quickly transferred to a display frame buffer without having to spend time determining from a Z buffer which frame buffer the image data should be retrieved from.

As per claim 5, Sakuraba teaches in Fig. 50 and in col. 28 lines 10-40 when disclosing the components of the drawing mechanism, an address register 438 including an offset address 440, an X address 442, and a Y address 444 used to access the Z buffer area 434 and the frame buffers 422,424, and 426. Sakuraba discloses that the XY addresses stored in the their respective registers correspond to the two-dimensional screen coordinates which "are used to designate the drawing address of the frame" (col. 28, lines 35-37). When image data stored in the frame buffers is accessed, the contents of the XY address registers 442 and 444 are sent to the frame control section 425, and the contents of the offset address register 440 are sent to a selector 446 to access a specific area of the Z buffer 434 corresponding to an individual display plane. The depth data z values stored in the Z buffer are eventually sent to a comparator 445, where the result of comparing the two z values are sent to the frame control section 435. These depth data z values are used to determine which frame memory should be accessed. The contents of the address register 434 specify to which frame memory and address the frame control section 428 will read from ("address register for storing the addresses of a plurality of storage areas in which the image data of each display face is stored"). Sakuraba teaches that image data stored in the frame buffer is read with the XY addresses stored in the address register 440, however, Sakuraba fails to teach that this address is selected based on information in the first register because Sakuraba's apparatus does not include such a register. Since Sakuraba does not expressly teach this first register; and Kurihara does not expressly teach an address register for storing the address of storage areas, Sakuraba and

Kurihara's teachings must be combined. As explained in the previous paragraph of this office action, Kurihara teaches a control register 26 used to store control bits that instruct which display plane is to be accessed, but the limited scope of Kurihara's disclosure fails to expressly teach the specifics of how image data is read from and written into the frame buffers 22 and 23.

It would have been obvious to one of ordinary skill in the art at the time to have incorporated Sakuraba's address register specifying which frame buffer and address to write to with Kurihara's control bits so that the control bits stored in the control register ("first register") specify which frame buffer to read/write to; and the address register specifies which address to write to ("address selected based on information of the first register").

As per claim 8, as discussed previously in paragraph 3 of this office action, Kurihara discloses a double buffering display unit comprising of a CPU 21, a frame buffer control circuit 25, a mask plane 41, and two frame buffers 22 and 23 corresponding to display planes A and B respectively. Within, the frame buffer control circuit 25, a control register 26 ("first register") stores control bits ("display switching enable bits"), which indicate the frame buffer or mask plane to be accessed. Once the first instruction indicating termination of generation of image data is received, the control bits are updated to indicate the frame memory or mask plane to be accessed next. The reasons for combining the teachings of Sakuraba, Kurihara and Recker remain the same as explained in paragraph 6 of this office action.

As per claims 9, 11, and 12, Sakuraba discloses that the three-dimensional drawing apparatus comprises a central processing unit 410 for managing the drawing data and window control of the device (col. 12 lines 45-47), a display control section 428 which reads out the superimposed image stored in the frame memory 426 and converts it into an analog signal for display output ("display control device for performing drawing processing and display control", "output display signals to a display device") (col. 27 lines 22-37), and a plurality of three-dimensional drawing mechanisms 22 responsible for calculating pixel interpolations ("plurality of display plane processing units each using image data") (Fig. 47 and col. 14 lines 52-57). As shown in Fig. 47 the drawing mechanisms 22 each include a frame buffer 800, 802, and 804 for storing display plane information ("image data of a plurality of display frames", "a memory"). Sakuraba teaches in Fig. 50 a three-dimensional drawing mechanism that contains an address register which is used to store addresses in the frame buffer memories as well as the Z buffer memory ("include a plurality of pieces of display information indicating storage destinations"). Similarly, Kurihara teaches in col. 4 lines 22-25 a mask plane 41 comprised of 1-bit data representing whether a screen pixel is stored in the first or second frame buffer. As shown in Fig. 9, after image data is read and written into a frame buffer (S62, S64) ("image generation") according to the new screen coordinates set in S42-S46, the control bits are reset to "00" (S65), thus activating the mask plane. The onset of the control bits being reset to "00" results in the mask plane to be updated with new mask plane data by reading and writing the 1-bit data to the mask plane according to the pixel's start and destination coordinates (S66) ("updating display

information...after receiving a first instruction indication of termination of drawing processing"). As previously discussed, the control bits serve as both an indicator and an instruction. The "00" control bits indicate the termination of generation of image data and instruct the mask plane to be updated (first instruction includes information for updating the display information"). Recker teaches in col. 5 lines 7-31 that the co-processor instructs the display controller 60 to switch between alternate frame buffers in order to avoid performance bottlenecks at the host processor and to prevent tearing of the displayed image. Recker teaches that the command to switch frame buffers does not necessarily have to be synchronized with the display timing. However, the subsequent display instructions are buffered while waiting for the frame buffers to switch so that they can be executed with the next vertical retrace. This double buffering alleviates the situation when a host processor cannot maintain the data transfer necessary for smooth video output. The host processor always writes to one buffer and a display controller always reads the other buffer. It is necessary for the frame buffers to be switched in synchronization to the vertical retrace so that a completely drawn image is displayed each time a frame buffer switch occurs. The reasons for combining the teachings of Sakuraba, Kurihara and Recker remain the same as explained in paragraph 6 of this office action.

As per claim 10, as discussed previously in paragraph 4 of this office action, Recker teaches a graphics system comprising of a co-processor connected to a display controller 60 via two frame buffers 40 and 50 in parallel, with the display controller then being connected to the display 70. Recker teaches in col. 5 lines 7-31 that the co-

processor instructs the display controller 60 to switch between alternate frame buffers in order to avoid performance bottlenecks at the host processor and to prevent tearing of the displayed image. Recker teaches that the command to switch frame buffers does not necessarily have to be synchronized with the display timing. However, the subsequent display instructions are buffered while waiting for the frame buffers to switch so that they can be executed with the next vertical retrace. This double buffering alleviates the situation when a host processor cannot maintain the data transfer necessary for smooth video output. The host processor always writes to one buffer and a display controller always reads the other buffer. It is necessary for the frame buffers to be switched in synchronization to the vertical retrace so that a completely drawn image is displayed each time a frame buffer switch occurs.

It would have been obvious to one of ordinary skill in the art at the time to incorporate Reckers' method of switching the frame buffers in sync with the display synchronization signal with the combined teachings of Sakuraba and Kurihara in order to create a display controller that can quickly transfer the data stored/updated in the frame buffers to a display frame buffer and can display images without tearing and flickering.

As per claim 13, Sakuraba teaches in Fig. 50 and in col. 28 lines 10-54 when disclosing the components of the drawing mechanism ("display plane processing unit"), an address register 438 including an offset address 440, an X address 442, and a Y address 444 ("display information") used to access the Z buffer area 434 and the frame buffers 422,424, and 426. Sakuraba discloses that the XY addresses stored in the their

respective registers correspond to the two-dimensional screen coordinates which "are used to designate the drawing address of the frame" (col. 28, lines 35-37). Sakuraba teaches that a CPU 410 generates the XYZ vertex coordinates of the polygon as well as the associated RGB pixel data before transferring it all to the drawing mechanism 420 via the main bus 412. Within the drawing mechanism, the XY coordinates are then stored in their respective registers ("display information...is capable of being updated at the same time"). In this embodiment, Sakuraba fails to teach a plurality of parallel drawing mechanisms processing image data for a plurality of display faces, however, a separate drawing mechanism embodiment described in col. 25 lines 32-40 and Fig. 47 and in col. 30-31, lines 42-19 teaches three drawing mechanisms executing pixel interpolation calculations in parallel in response to the first instruction being executed by the display control device. Kurihara teaches in Fig. 2A, Fig. 2C, cols. 4-5 lines 45-4 and col. 5, lines 4-46 that the control register 26 ("a first register") included within the frame buffer control circuit 26 is used to store the control bits (b1 b0) ("display enable bits") indicating the frame buffer or mask plane to be accessed and that control bits (1 1) indicates that both frame buffer 22 (display plane A) and frame buffer 23 (display plane B) are both accessed simultaneously. A control signal based on the control bits is then output to the frame buffers via control bus 36 and 42 ("setting of switching...is performed based on the display switching enable bits"). A data register 33 has a capacity of 49 bits so that the image data for the first frame buffer 22, the second frame buffer 23 and the 1-bit data for the mask plane can be simultaneously stored indicating that two or more pieces of the display information used in the display plane processing

units is capable of being updated at the same time in response to the first instruction being executed by the display control device. The reasons for combining the teachings of Sakuraba, Kurihara and Recker remain the same as explained in paragraph 6 of this office action.

Claim 15 is similar in scope to claim 1, and is rejected under the same rationale. However, the claim limitation of "image data further subjected to superimposing processing" can be interpreted to mean that image data is subjected to superimposing after being read by the display processing circuit; or that superimposed image data is subject to additional superimposing. Further clarification is needed in order for the claim to follow the provided specification. Sakuraba teaches in col. 29 lines 56-61 that after the superimposed image data is written into another frame memory, it is transferred to the display control section 428, where it is converted into analog output signals. Sakuraba does not expressly teach recycling previously superimposed image data.

As per claim 16, Sakuraba teaches the switching of frame buffers is determined by comparing the depth data z values, but Sakuraba fails to expressly teach of a setting made to indicate whether or not a storage area is to be switched.

Kurihara discloses a double buffering display unit comprising of a CPU 21, a frame buffer control circuit 25, a mask plane 41, and two frame buffers 22 and 23 corresponding to display planes A and B respectively. With conventional double buffering, image data is stored in the first and second buffers and a display controller reads from one buffer or the other. However, Kurihara teaches in col. 4 lines 22-25 an additional mask plane storing 1-bit data per pixel indicating whether the associated

image data is located in the first or second frame buffer ("setting is made whether or not a storage area from which the image data is read is switched for each display face"). By initially storing which frame buffer the image data is stored in, the time required to transfer this image data to a display frame buffer is reduced because the location (first or second frame buffer) of this image data does not have to be determined. In Fig. 9, Kurihara teaches that after image data is read and written into a frame buffer (S62, S64) according to the new screen coordinates set in S42-S46, 1-bit pixel data is read from and written to the mask plane according to the pixel's start and destination coordinates (S66) ("setting made...at termination of generation of image data"). Kurihara teaches in Fig. 2A, Fig. 2C, col. 5 lines 4-46 that the control register 26 ("a first register") included within the frame buffer control circuit 26 is used to store the control bits (b1 b0) ("display enable bits") indicating the frame buffer or mask plane to be accessed. A control signal based on the control bits is then output to the frame buffers via control bus 36 and 42 ("setting of switching...is performed based on the display switching enable bits"). Kurihara does not expressly teach a one-to-one correspondence between each of the control bits ("display enable bits") and a display face. However, the control bits serve as operation codes for switching to the frame buffers and mask plane. In Fig. 9, Kurihara teaches that the process of controlling the frame buffers in order to generate new image data for output consists of setting the control bits in the control registers (S61, S63, S65) and reading and writing image data into the frame buffers on a per-pixel basis. The figure illustrates with S61 and S63 that after setting the control bits in the control register corresponds to switching to either the first or second frame buffer ("setting of switching

to a storage area...is performed by updating the first register"). Kurihara's method and apparatus provides a way of initially storing an indication of which frame buffer image data is stored in. It would have been obvious to replace Sakuraba's depth data control mechanism for determining which frame buffer to access with Kurihara's method and apparatus so that data stored in the frame buffers can be quickly transferred to a display frame buffer without having to spend time determining from a Z buffer which frame buffer the image data should be retrieved from.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,757,455 to Tsunoda et al. in view of U.S. Patent No. 5,850,224 to Sakuraba, U.S. Patent No. 6,005,572 to Kurihara, and U.S. Patent No. 5,657,478 to Recker et al.

As per claim 14, Tsunoda teaches a navigation system for a vehicle in Fig. 1, col. 5 lines 50-55, col. 6 lines 3-14, and lines 20-22 comprising of a display CPU 33 programmed to generate display images ("generating the series of commands executed by the display control device or data"), a Random Access Memory (RAM) 43 which stores the final imaged to be displayed ("memory unit for storing image data generated by the display control device"), a display unit ("display device"), a Read-Only Memory (ROM) card 28 which "permanently stores the map data" ("memory device for storing map information"), and an encompassing display control circuit 32 ("display control device"). The claimed central processing unit is external to the display control device,

however Tsunoda incorporates this CPU within the display control device itself. The functionality of the processor is the same in that the CPU receives image data and generates the commands necessary for output. A separate map calculating CPU 30 exists for calculating vehicle position based on sensor input. The display CPU 33 would receive map data from the map calculating CPU 30 and issue the necessary commands to the output display unit 36. Although Tsunoda does teach a display control circuit 32 within the navigation system, it does not comprise of the same components in the claimed display control device. Sakuraba, Kurihara and Recker address the limitations pertaining to the display control device in paragraphs 3-6 of this office action. The reasons for combining the teachings of Sakuraba, Kurihara and Recker remain the same as explained in paragraph 6 of this office action. It would have been obvious to one of ordinary skill in the art at the time to have incorporated Sakuraba, Kurihara and Recker's display control device into Tsunoda's navigation system in order to allow optimum display switching in an application where there are limited resources available.

Response to Arguments

Applicant's arguments filed 3/20/2007 have been fully considered but they are not persuasive. Applicant argues, with respect to claim 1, "...However, Sakuraba does not show or suggest, either explicitly or implicitly, that the frame buffer is switched according to vertical synchronous signal of the color display. Furthermore, because, as recited in claim 1, the display processing unit is operable to switch the storage areas from which the image data is read according to the display switching information, the

storage area in the display control device recited in claim 1 is switched to selectively read out the data to display an image. In contrast, Sakuraba merely shows that a plurality of frame memories 422, 424 and 426 are coupled to the three dimensional drawing mechanism 420 and a display control section 428, and data from the frame buffer is displayed to the color display read out by the display control section 428 (Fig. 49, col. 27, lines 18-36). Sakuraba does not show or suggest explicitly or implicitly that the frame buffer is switched by the display control section 428 to selectively read out data to display the color display 430...", "...Kurihara does not show or suggest, either explicitly or implicitly, switching a frame buffer to readout the image data in order to display an image on the screen. Clearly, Kurihara cannot show or suggest, either explicitly or implicitly, switching a frame buffer according to a vertical synchronous signal of the screen unit..." and "...The secondary reference of Recker shows a system that includes a host, a co\-processor and a display. In Recker, the host sends a command for performing a display switch to a FIFO command buffer, and the co-processor receives the command for performing a display switch from the FIFO command buffer and executes the command for performing a display switch (col. 4, line 61- col. 5, line 6). The display is switched by switching a second frame buffer to a first frame buffer according to execution of the display switch command (step 385 in Fig. 3) and accessing the first frame buffer to display an image. In other words, Recker's system switches frame buffers to be accessed only according to the execution of the command for switching a display by the co-processor. Recker does not show or suggest either explicitly or implicitly that a display can switch a frame buffer according to a

vertical synchronous signal of the display. Therefore, the secondary reference of Recker fails to provide any disclosure, teaching or suggestion that makes up for the deficiencies in Sakuraba and Kurihara, as set forth above. Accordingly, claim 1 is not obvious over Sakuraba, Kurihara and Recker...".

Examiner respectfully submits that Recker teaches wherein the co-processor is instructed to wait until the beginning or end of the vertical blanking signal to perform the frame buffer switches for rendering and display such that the co-processor does not execute any commands received from the processor until the frame buffers are switched by the display switch command at the beginning of the vertical blanking interval, see column 2, lines 50-67 and column 4, lines 4-40, thus the limitation "wherein the display processing unit is operable to switch the storage areas from which the image data is read are capable of switching for each display face by the display processing circuit according to the display switching information, in response to the display control device receiving a display vertical synchronous signal of a display device" is disclosed since it is understood that the signal indicating the beginning of the next vertical blanking interval is a vertical synchronous signal indicating a vertical retrace interval.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberta Prendergast whose telephone number is (571) 272-7647. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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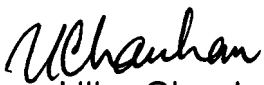

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